In the Claims:

Please cancel claims 9-11, and 20-22.

1-6. (canceled)

7(previously presented).   A packet processor comprising:

a plurality of logical blocks, each of said plurality of logical blocks includes a sub-processor, said plurality of logical blocks pipelined in series with each other, each of said plurality of logical block operating independently of each other allowing concurrent processing of said plurality of sub-processors;

each of said plurality of logical blocks further including

an input receiving a first packet data associated with a first packet and a second packet data associated with a second packet;

a storage device storing the first packet data and the second packet data;

said sub-processor coupled to the storage device, the sub-processor switching from processing the first packet data to processing the second packet data while awaiting a processing result for the first packet data.

8(original).   The packet processor of claim 7, wherein the processing result is a conditional branch instruction result.

9-22 (canceled)

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